Assignment 3 report

Real-time Operating System - 48450

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Note: This is a guide template to help you complete the assignment. There will be no penalty on your assignment score if you do not use this template. You are welcome to design your own template for the assignment.

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1. Introduction

In this section, an introduction about the assignment is presented and some core technical knowledge that you will use are highlighted.

This assignment is a topic about CPU scheduling and Memory management, which are key elements in Real Time Operating System. This report covers the Theory of operation- highlighting and defining the key concepts used in this assignment. This is then followed by the operating condition which describes the high-level functioning and interaction between the different components. The practical application from theory to code follows in the implementation section. This is then followed by the experimental results of the final code to test with the specification. The report concludes with an analysis of the results.

1. Theory of operation

In this section, the brief but clear explanations about the technical knowledge are given for this assignment. For example, the theory, the functions and the usage etc.

1. CPU scheduling and Memory management

CPU scheduling is the basis of multiprogrammed operating systems. By switching the CPU among processes, the operating system can make the computer more productive.

To maximize CPU utilization, the idea is relatively simple. A process is executed until it must wait, typically for the completion of some I/O request. In a simple computer system, the CPU then just sits idle. All this waiting time is wasted; no useful work is accomplished. With multiprogramming, we try to use this time productively. Several processes are kept in memory at one time. When one process has to wait, the operating system takes the CPU away from that process and gives the CPU to another process. [OPERATING SYSTEM CONCEPTS 261-2]

1. FIFOs

The ﬁrst in, ﬁrst out (FIFO) principle: items are removed from a queue in the order in which they were inserted. There are many everyday examples of queues, including shoppers waiting in a checkout line at a store and cars waiting in line at a trafﬁc signal [OPERATING SYSTEM CONCEPTS 32]

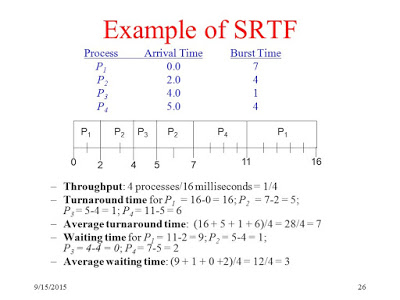
1. Signal concepts

A signal is used in UNIX systems to notify a process that a particular event has occurred. A signal may be received either synchronously or asynchronously. [OPERATING SYSTEM CONCEPTS 183]

1. Shortest-remaining-time-first algorithm (SRTF)

CPU scheduling deals with the problem of deciding which of the processes in the ready queue is to be allocated the CPU. There are many different CPU-scheduling algorithms. In this section, SRTF is described.

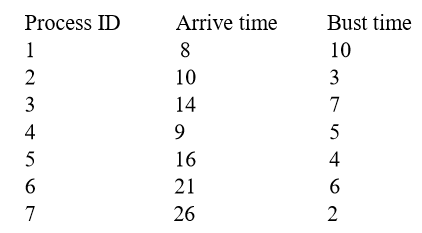
This algorithm associates with each process the length of the process’s next CPU burst. When the CPU is available, it is assigned to the process that has the smallest next CPU burst. If the next CPU bursts of two processes are the same, FCFS (first come first served) scheduling is used to break the tie. Note that a more appropriate term for this scheduling method would be the shortest-next CPU-burst algorithm, because scheduling depends on the length of the next CPU burst of a process, rather than its total length. [OPERATING SYSTEM CONCEPTS 268-70]



[http://dotclu.blogspot.com.au/2017/11/shortest-remaining-time-first-srtf.html]

1. Operating condition

In this section, a summary about your understanding of the assignment is given. In order to complete the assignment, you might give a summary about key points that the assignment contains. In addition, you might explain the relationships between these points.



The specific application of SRTF algorithm for this assignment is as follows

| Time | Process Time Remaining | | | | | | | | ACTIVE Process | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Process 1 | Process 2 | Process 3 | Process 4 | Process 5 | Process 6 | Process 7 |  | |
| 0-7 | Not Arrived | Not Arrived 3 units remaining | Not Arrived 7 units remaining | Not Arrived | Not Arrived 4 units remaining | Not Arrived 6 units remaining | Not Arrived 2 units remaining | None | |
| 10 units remaining | 5 units remaining |
| 8 | ACTIVE | Not Arrived 3 units remaining | Not Arrived 7 units remaining | Not Arrived | Not Arrived 4 units remaining | Not Arrived 6 units remaining | Not Arrived 2 units remaining | Process 1 | |
| 9 units | 5 units remaining |
| remaining |  |
| 9 | Arrived | Not Arrived 3 units remaining | Not Arrived 7 units remaining | ACTIVE | Not Arrived 4 units remaining | Not Arrived 6 units remaining | Not Arrived 2 units remaining | Process 4 | |
| 9 units | 4 units remaining |
| remaining |  |
| 10 | Arrived | ACTIVE | Not Arrived 7 units remaining | Arrived | Not Arrived 4 units remaining | Not Arrived 6 units remaining | Not Arrived 2 units remaining | Process 2 | |
| 9 units | 2 units remaining | 4 units remaining |
| remaining |  |  |
| 11 | Arrived | ACTIVE | Not Arrived 7 units remaining | Arrived | Not Arrived 4 units remaining | Not Arrived 6 units remaining | Not Arrived 2 units remaining | Process 2 | |
| 9 units | 1 units remaining | 4 units remaining |
| remaining |  |  |
| 12 | Arrived | ACTIVE | Not Arrived 7 units remaining | Arrived | Not Arrived 4 units remaining | Not Arrived 6 units remaining | Not Arrived 2 units remaining | Process 2 | |
| 9 units | 0 units remaining | 4 units remaining |
| remaining |  |  |
| 13 | Arrived | Complete t = 13 | Not Arrived 7 units remaining | ACTIVE | Not Arrived 4 units remaining | Not Arrived 6 units remaining | Not Arrived 2 units remaining | Process 4 | |
| 9 units | 3 units remaining |
| remaining |  |
| 14 | Arrived | Complete t = 13 | Arrived | ACTIVE | Not Arrived 4 units remaining | Not Arrived 6 units remaining | Not Arrived 2 units remaining | Process 4 | |
| 9 units | 7 units remaining | 2 units remaining |
| remaining |  |  |
| 15 | Arrived | Complete t = 13 | Arrived | ACTIVE | Not Arrived 4 units remaining | Not Arrived 6 units remaining | Not Arrived 2 units remaining | Process 4 | |
| 9 units | 7 units remaining | 1 unit remaining |
| remaining |  |  |
| 16 | Arrived | Complete t = 13 | Arrived | ACTIVE | Arrived | Not Arrived 6 units remaining | Not Arrived 2 units remaining | Process 4 | |
| 9 units | 7 units remaining | 0 units remaining | 4 units remaining |
| remaining |  |  |  |
| 17 | Arrived | Complete t = 13 | Arrived | Complete t = 17 | ACTIVE | Not Arrived 6 units remaining | Not Arrived 2 units remaining | Process 5 | |
| 9 units | 7 units remaining | 3 units remaining |
| remaining |  |  |
| 18 | Arrived | Complete t = 13 | Arrived | Complete t = 17 | ACTIVE | Not Arrived 6 units remaining | Not Arrived 2 units remaining | Process 5 | |
| 9 units | 7 units remaining | 2 units remaining |
| remaining |  |  |
| 19 | Arrived | Complete t = 13 | Arrived | Complete t = 17 | ACTIVE | Not Arrived 6 units remaining | Not Arrived 2 units remaining | Process 5 | |
| 9 units | 7 units remaining | 1 unit remaining |
| remaining |  |  |
| 20 | Arrived | Complete t = 13 | Arrived | Complete t = 17 | ACTIVE | Not Arrived 6 units remaining | Not Arrived 2 units remaining | Process 5 | |
| 9 units | 7 units remaining | 0 units remaining |
| remaining |  |  |
| 21 | Arrived | Complete t = 13 | Arrived | Complete t = 17 | Complete t = 21 | ACTIVE | Not Arrived 2 units remaining | Process 6 | |
| 9 units | 7 units remaining | 5 units remaining |
| remaining |  |  |
| 22 | Arrived | Complete t = 13 | Arrived | Complete t = 17 | Complete t = 21 | ACTIVE | Not Arrived 2 units remaining | Process 6 | |
| 9 units | 7 units remaining | 4 units remaining |
| remaining |  |  |
| 23 | Arrived | Complete t = 13 | Arrived | Complete t = 17 | Complete t = 21 | ACTIVE | Not Arrived 2 units remaining | Process 6 | |
| 9 units | 7 units remaining | 3 units remaining |
| remaining |  |  |
| 24 | Arrived | Complete t = 13 | Arrived | Complete t = 17 | Complete t = 21 | ACTIVE | Not Arrived 2 units remaining | Process 6 | |
| 9 units | 7 units remaining | 2 units remaining |
| remaining |  |  |
| 25 | Arrived | Complete t = 13 | Arrived | Complete t = 17 | Complete t = 21 | ACTIVE | Not Arrived 2 units remaining | Process 6 | |
| 9 units | 7 units remaining | 1 unit remaining |
| remaining |  |  |
| 26 | Arrived | Complete t = 13 | Arrived | Complete t = 17 | Complete t = 21 | ACTIVE | Arrived | Process 6 | |
| 9 units | 7 units remaining | 0 units remaining | 2 units remaining |
| remaining |  |  |  |
| 27 | Arrived | Complete t = 13 | Arrived | Complete t = 17 | Complete t = 21 | Complete t = 27 | ACTIVE | Process 7 | |
| 9 units | 7 units remaining | 1 unit remaining |
| remaining |  |  |
| 28 | Arrived | Complete t = 13 | Arrived | Complete t = 17 | Complete t = 21 | Complete t = 27 | ACTIVE | Process 7 | |
| 9 units | 7 units remaining | 0 units remaining |
| remaining |  |  |
| 29 | Arrived | Complete t = 13 | ACTIVE | Complete t = 17 | Complete t = 21 | Complete t = 27 | Complete t = 29 | Process 3 | |
| 9 units | 6 units remaining |
| remaining |  |
| 30 | Arrived | Complete t = 13 | ACTIVE | Complete t = 17 | Complete t = 21 | Complete t = 27 | Complete t = 29 | Process 3 | |
| 9 units | 5 units remaining |
| remaining |  |
| 31 | Arrived | Complete t = 13 | ACTIVE | Complete t = 17 | Complete t = 21 | Complete t = 27 | Complete t = 29 | Process 3 | |
| 9 units | 4 units remaining |
| remaining |  |
| 32 | Arrived | Complete t = 13 | ACTIVE | Complete t = 17 | Complete t = 21 | Complete t = 27 | Complete t = 29 | Process 3 | |
| 9 units | 3 units remaining |
| remaining |  |
| 33 | Arrived | Complete t = 13 | ACTIVE | Complete t = 17 | Complete t = 21 | Complete t = 27 | Complete t = 29 | Process 3 | |
| 9 units | 2 units remaining |
| remaining |  |
| 34 | Arrived | Complete t = 13 | ACTIVE | Complete t = 17 | Complete t = 21 | Complete t = 27 | Complete t = 29 | Process 3 | |
| 9 units | 1 unit remaining |
| remaining |  |
| 35 | Arrived | Complete t = 13 | ACTIVE | Complete t = 17 | Complete t = 21 | Complete t = 27 | Complete t = 29 | Process 3 | |
| 9 units | 0 units remaining |
| remaining |  |
| 36 | ACTIVE | Complete t = 13 | Complete t = 38 | Complete t = 17 | Complete t = 21 | Complete t = 27 | Complete t = 29 | Process 1 | |
| 8 units |
| remaining |
| 37 | ACTIVE | Complete t = 13 | Complete t = 38 | Complete t = 17 | Complete t = 21 | Complete t = 27 | Complete t = 29 | Process 1 | |
| 7 units |
| remaining |
| 38 | ACTIVE | Complete t = 13 | Complete t = 38 | Complete t = 17 | Complete t = 21 | Complete t = 27 | Complete t = 29 | Process 1 | |
| 6 units |
| remaining |
| 39 | ACTIVE | Complete t = 13 | Complete t = 38 | Complete t = 17 | Complete t = 21 | Complete t = 27 | Complete t = 29 | Process 1 | |
| 5 units |
| remaining |
| 40 | ACTIVE | Complete t = 13 | Complete t = 38 | Complete t = 17 | Complete t = 21 | Complete t = 27 | Complete t = 29 | Process 1 | |
| 4 units |
| remaining |
| 41 | ACTIVE | Complete t = 13 | Complete t = 38 | Complete t = 17 | Complete t = 21 | Complete t = 27 | Complete t = 29 | Process 1 | |
| 3 units |
| remaining |
| 42 | ACTIVE | Complete t = 13 | Complete t = 38 | Complete t = 17 | Complete t = 21 | Complete t = 27 | Complete t = 29 | Process 1 | |
| 2 units |
| remaining |
| 43 | ACTIVE | Complete t = 13 | Complete t = 38 | Complete t = 17 | Complete t = 21 | Complete t = 27 | Complete t = 29 | Process 1 | |
| 1 unit |
| remaining |
| 44 | ACTIVE | Complete t = 13 | Complete t = 38 | Complete t = 17 | Complete t = 21 | Complete t = 27 | Complete t = 29 | Process 1 | |
| 0 units |
| remaining |
| 45 | Complete  t = 45 | Complete t = 13 | Complete t = 38 | Complete t = 17 | Complete t = 21 | Complete t = 27 | Complete t = 29 | None | |

A summary is presented below

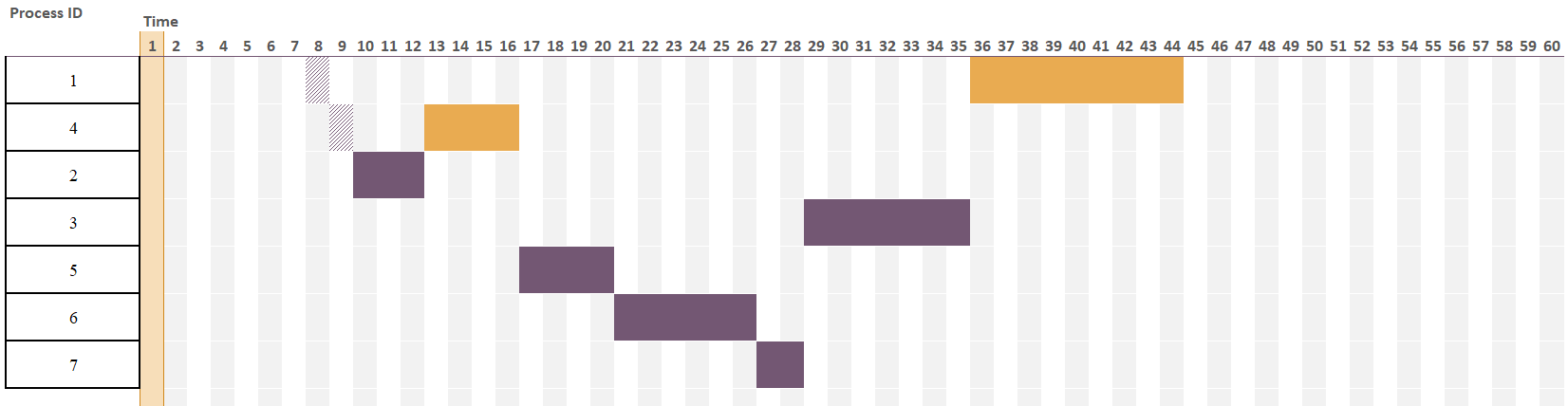
Sequence: P1 🡪 P4 🡪P2 🡪 P4 🡪P5 🡪 P6 🡪P7 🡪 P3🡪 P1

|  |  |  |  |
| --- | --- | --- | --- |
| Process ID | Arrival Time | Burst Time | Completion Time |
| 1 | 8 | 10 | 45 |
| 2 | 10 | 3 | 13 |
| 3 | 14 | 7 | 38 |
| 4 | 9 | 5 | 17 |
| 5 | 16 | 4 | 21 |
| 6 | 21 | 6 | 27 |
| 7 | 26 | 2 | 29 |

We are now able to sort by arrival time to calculate the parameters and determine the Gantt Chart

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Process ID | Arrival Time | Burst Time | Completion Time | Turn Around Time (TAT) =Completion - Arrival | Waiting Time  = TAT  - Burst |
| 1 | 8 | 10 | 45 | 37 | 27 |
| 4 | 9 | 5 | 13 | 4 | -1 |
| 2 | 10 | 3 | 38 | 28 | 25 |
| 3 | 14 | 7 | 17 | 3 | -4 |
| 5 | 16 | 4 | 21 | 5 | 1 |
| 6 | 21 | 6 | 27 | 6 | 0 |
| 7 | 26 | 2 | 29 | 3 | 1 |
| AVERAGE |  |  |  | 12.28571429 | 7 |

Sequence: P1 🡪 P4 🡪P2 🡪 P4 🡪P5 🡪 P6 🡪P7 🡪 P3🡪 P1



P7 End t = 29

P6 End t = 27

P7 End t = 36

P6 Start t = 21

P5 End t = 21

P3 End t = 36

P3 Start t = 29

P1 End t = 45

P4 End t = 17

P5 Start t = 17

P2 End t = 13

P2 Start t = 10

P4 Start t = 9

P1 Start t = 8

1. Implementation
2. Method

In this section, you might list how you solve the problem and how you complete your program. You might write your software design strategy about your programing.

1. Flow chart

The flow chart about this assignment is shown below.

1. Experiments
2. Hypothesis

Give an explanation about the experiment questions. If there are no questions, just omit this part.

1. Results

For demonstration purpose, you might give some graphs about your program running. An example is shown below.

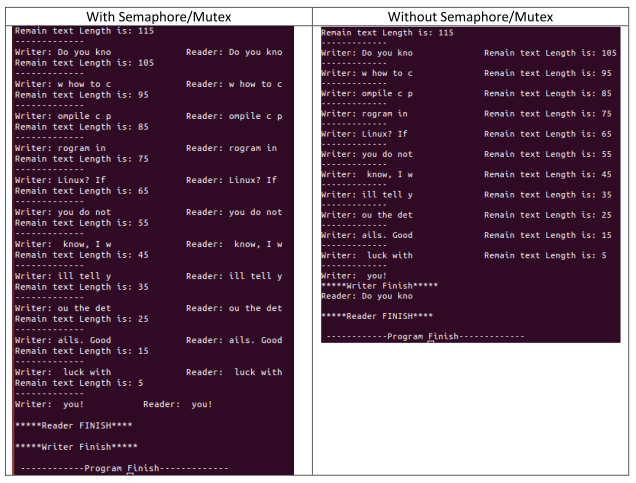


Figure 1. Experimental results with and without semaphore/mutex.

1. Conclusion on result analysis

If this is a simple report assignment, you might give a brief conclusion related this assignment.

If this is a report assignment, you might carefully observe the output of your program and give some explanations and analysis about the output/performance/outcomes based on our understanding.

1. References

If you have references, please referee it correctly.

A. Silberschatz, P. B. Galvin & G. Gagne, 2012, Operating System Concepts, 9 th edn, John Wiley & Sons, New York.